Flip Chip CSP

fcCSP, fcLGA, fcPoP-MLP, Interposer PoP, Bare Die fcPoP, fcCSP Hybrid

Highlights

- A complete portfolio of high to low-end fcCSP packages for all mobile applications, including fcCSP, fcLGA, flip chip package-on-package (bare die PoP and molded laser PoP), interposer PoP, and hybrid flip chip/wirebond solutions
- A leader in the development of a broad range of low cost substrate and process technologies for the cost sensitive mobile and consumer market
- Ultra low flip chip interconnect parasitic eliminates wire inductance and resistance compared to wirebond interconnect
- One piece heat spreader can be added for exceptional thermal performance

Features

- Body sizes 3 x 3mm through 17 x 19mm
- Electroplated Pb-free or Cu pillar bumps
- Bumping capability down to 130µm pitch with lead-free solder and pitch down to 40µm with Cu pillar
- Full service wafer bumping with PBO and PI dielectric options for wafer repassivation and redistribution layer (RDL)
- Molded underfill (MUF) or Capillary underfill (CUF) options
- Uniquely developed fcCuBE® Mass Reflow (MR) process supports bump pitches down to 80µm and below, providing a lower cost alternative to Thermal-Compression Bonding (TCB)
- Thermal-Compression Bonding with Non-conductive Paste (TCNCP) available
- MUF with solder bump and Cu pillar qualified and in production
- 140µm minimum die solder bump pitch in production
- BGA/LGA pitch down to 0.30mm qualified and 0.35mm in production
- Maximum overall height of 1.40mm (fcLCSP); 1.20mm (fcTCSP); 1.00mm (fcVCSP); 0.65mm (fcLGA)
- Minimum Z height fcCSP hybrid package qualified 0.55mm, and 0.6mm in production
- Conventional 2 to 6 layer through-hole or PPG build-up laminate substrates available; ABF build-up substrates available
- Low cost substrate technology options including Embedded Trace Substrate (ETS), Molded Interconnect Substrate (MIS) in HVM, and Via Under Trace (VUT) qualified, No-Clean Flux and Non-PI Bumping qualified and HVM, and others such as large die CUF and Land Side Cap (LSC) with 0.4mm BGA pitch, Embedded Passive Substrate (EPS) in HVM
- One piece heat spreader option for exceptional thermal performance; fcCSP-ED-H (1-piece heat spreader) with MUF in high volume production
- Packages assembled in either bare die, exposed die and overmolded strip matrix format, and saw singulated; ultra high density wide strip available

Our fcCSP packages form a subgroup of the Flip Chip package family of the form factor known as Chip Scale Packages (CSP). We offer a complete fcCSP portfolio of high to low-end leading edge packages for all mobile applications including standard fine pitch fcCSP packages, hybrid flip chip and fcPoP including Bare Die fcPoP, Interposer POP and Molded Laser PoP (fcPoP MLP).

Our standard fcCSP packages include very thin profile packages (fcTCSP, fcVCSP, fcWCSP and fcUCSP), as well as side-by-side die configurations. All fcCSP packages are produced on substrates with matrix strip format and use overmolding and saw singulation processes similar to wirebond packages of the same form factors. The fcCSP is an overmolded package with solder balls, and is available in a high thermal performance package (fcCSP-H) produced on substrates in matrix strip format with heat spreader.

fcCSP packages are also available in very thin profile hybrid flip chip (flip chip on the bottom and wirebond die on the top) such as fcTCSP-SD2 and fcTCSP-SD3. Hybrid fcCSP packages are available with Mass Reflow (MR), CUF or MUF, and copper (Cu) pillar and Cu wire.

Our fcCSP offering also includes package-on-package (PoP) solutions in Bare Die and Molded Laser formats. Both fcPoP formats are offered as the bottom PoP package (PoPb) of a stackable flip chip BGA. PoPb is typically an application processor or an integrated baseband device with land pads placed on the top periphery of the package surface to enable the stacking of a second CSP or PoP top (PoPt) above.

Bare Die PoP differs from fcCSP through the inclusion of memory interface (MI) pads on the substrate top side. Molded Laser PoP (MLP) offers aggressive package height reductions or 0.35mm MI pitch, and, with its overmold configuration, provides better warpage performance. MLP-PoP is also offered with an exposed die (ED) which reduces mold cap height and improved warpage performance.

Applications

We offer a complete fcCSP portfolio of high to low-end packages for all mobile applications:

- Mobile processors for Smart Phones, Tablets and Wearable Electronic (WE) devices including baseband, application processors, and application processors + baseband
- Chipsets for peripheral IC's driven by demand for high-end Smart Phone functionality, including RFIC, PMIC, Connectivity, Sensors/ MEMS, and Audio CODEC

Specifications

Package Thickness	0.55mm - 1.4mm
Die Thickness	250mm - 60mm
Minimum Bump Pitch	130mm, lead-free solder 40mm, Cu pillar
Marking	Laser

Reliability

Moisture Sensitivity Level	JEDEC Level 3 @ 260°C
Temperature Cycling	-55°C/125°C, 1000 cycles (typical)
High Temperature Storage	150°C, 1000 hrs (typical)
Unbiasted HAST	130°C, 85% RH, 2 atm, 96 hrs (typical)

Thermal Performance

Thermal performance is highly dependent on package size, die size, substrate layers and thickness, and solder ball configuration. Simulation for specific applications should be performed to obtain maximum accuracy.

Package	Body Size (mm)	Pin Count	Die Size (mm)	Thermal Performance ja θ°C/W
fcCSP	7 x 7	191	4.46 x 5.65	33.2
fcLCSP-H*	14 x 14	425	4.9 x 4.9	14.0

Notes: Simulation data for package mounted on 4 layer PCB (per JEDEC JESD51-9) under natural convection as defined in JESD51-2. *H/S: 0.3mm formed "Hat" type; 100um TIM1 and 100um lid adhesive: 1.75W/mK.

Electrical Performance

Electrical parasitic data is highly dependent on the package layout. 3D electrical simulation can be used on the specific package design to provide the best prediction of electrical behavior. First order approximations can be calculated using parasitics per unit length for the constituents of the signal path. Data below is for a fcLCSP package, body size 13 x 13mm, 6.0 x 8.0mm die size and frequency of 100MHz.

Length	Inductance (nH)	Capacitance (pF)	Resitance (mΩ)
Self (short)	0.89	0.65	18.3
Mutual	0.24	0.11	
Self (long)	1.78	0.73	32.5
Mutual	0.51	0.12	

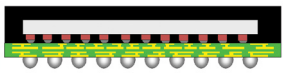
Note: Net = Total Trace Length + Via + Solder Ball.

Cross Sections

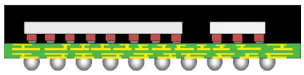
fcCSP

Market: Smart Phone & Tablets AP+BB processors and BB; Chipsets (RFIC, PA, XCVR, PMIC, Connectivity, etc)

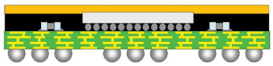
fcVCSP
Very thin profile package



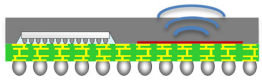
fcVCSP-SS2
Very thin profile, 2 die side by side package



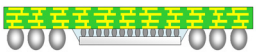
fcCSP-ED-H
Fine pitch, exposed die with heat spreader



fcCSP-AiP
Antenna-in-package for 5G and wireless



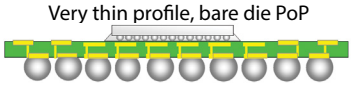
fcCSP-AiP (Marsupial)
Antenna-in-package for 5G and wireless



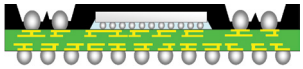
fcPoP

Market: Smart Phones
AP Processors (AP, AP+BB)

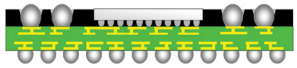
fcVSCP-PoP
Very thin profile, bare die PoP



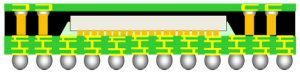
fcVCSP-MLP PoP
Very thin profile, molded laser PoP



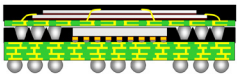
fcVCSP MLP PoP-ED
Very thin profile, molded laser, exposed die PoP



fcVCSP Interposer PoP
Very thin profile, interposer PoP



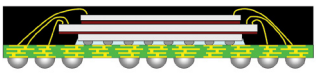
fcVCSP Interposer PoP with TIM
Very thin profile, interposer die PoP



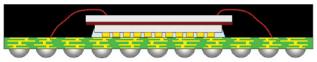
HYBRIDS

Market: Smart Phones & Wearables
BB / Modem; BB + Memory + PMU;
MCU/ AP + BT+ Sensors (WE)

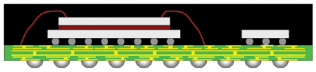
fcVCSP-Hybrid w/CUF
Very thin profile hybrid Wirebond - Flip Chip



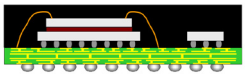
fcWCSP-Hybrid Fine Pitch Cu Pillar
Very very thin profile hybrid Wirebond - Flip Chip



fcVCSP Hybrid-SS2, Cu wire
Very thin profile, 2 die side by side, stacked hybrid MUF



fcVCSP Hybrid-SS2, Ag wire
Very thin profile, 2 die side by side, stacked hybrid MUF



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